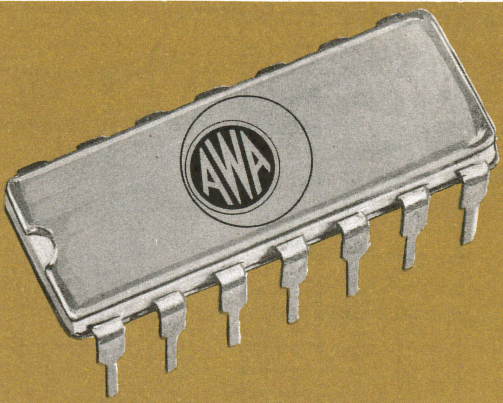
INTEGRATED CIRCUIT

AWM 1268

FOUR BIT MEMORY

Serial in, parallel out.



14 Lead Dual-in-Line ceramic package.
Details on Page 4.

The AWM1268 is a DTL MSI functional block incorporating a four bit store.

Data from a common input line is written into a location by applying a logic zero to the corresponding write clock line. Data entry is edge triggered on the negative-going transition of the clock pulse and is provided by a master-slave flip-flop.

Individual data read-out of the four cells is provided and the output of each is buffered into an open collector output stage which provides a wired-OR capability..

The outputs may be read from each cell independently of the data entry.

APPLICATIONS

- Fast access data stores.
- Multiplexer – Demultiplexers.
- Serial – Parallel data conversion.

FEATURES

- Wired-OR capability

GENERAL CHARACTERISTICS

Package	14 lead hemitic Dual-in-Line ceramic
Maximum Storage Temperature	140°C
Operating Temperature Range	0°C to 70°C
Supply Voltage Range	4.5 to 5.5 volts
Maximum Input to any Pin	+5.5 volts
Minimum Input to any Pin	–0.5 volt
Logic Levels	Compatible with TTL/DTL
Fan Out (Per line)	2 Standard loads
Write Cycle Time	45 nS (typical)
Power Dissipation	150 milliwatts

Designed and Manufactured in Australia by –

AMALGAMATED WIRELESS (AUSTRALASIA) LTD.
348 Victoria Road Rydalmere N.S.W. Australia.
Postal Address – A.W.V. Private Mail Bag Ermington, 2115
Telegrams "Valves" Ermington, Telephone 638 0411.

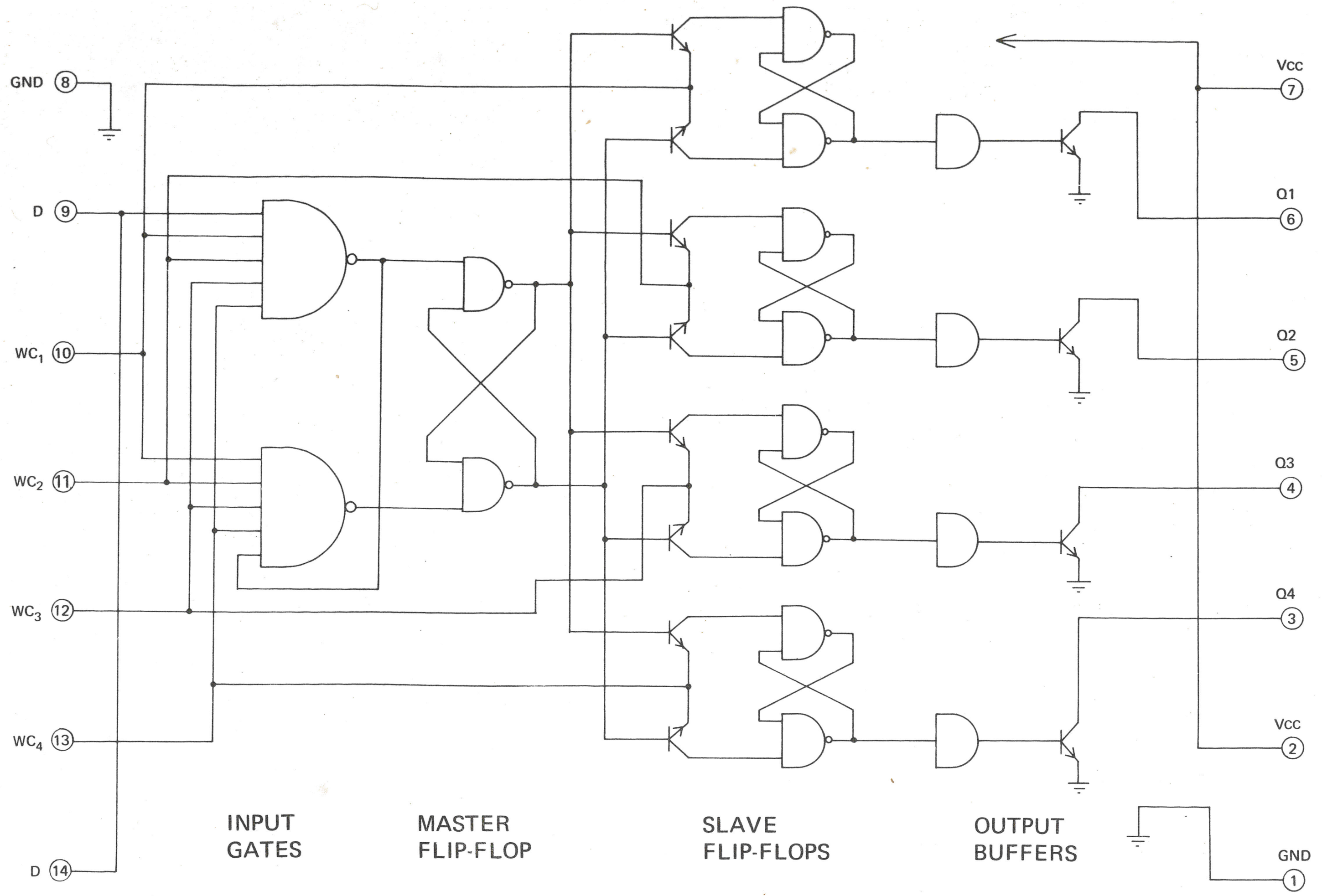


Figure 1. AWM1268 Functional schematic diagram

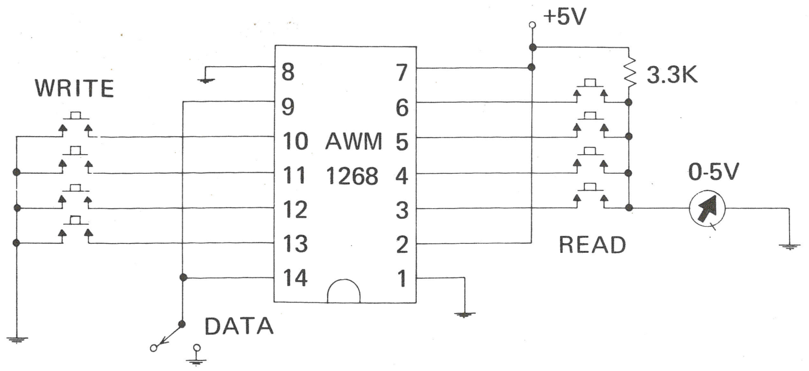


Figure 2

Functional Test Set-Up

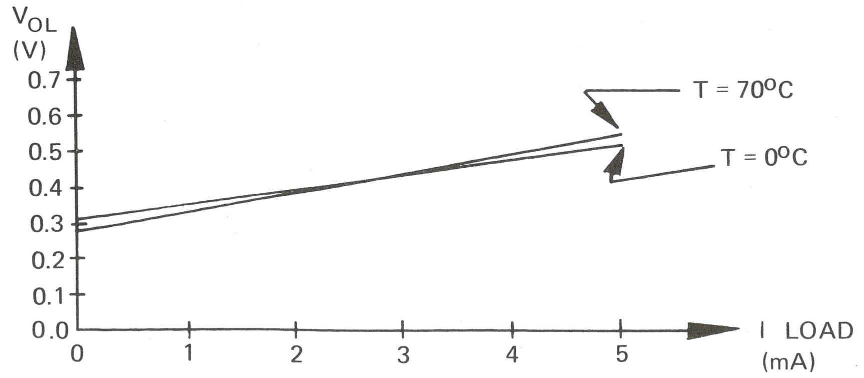


Figure 3

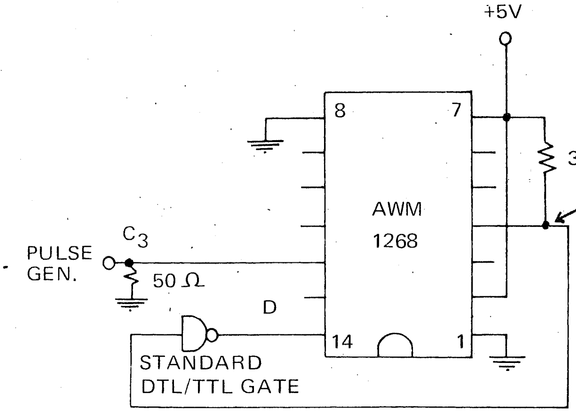
Output Loading Curve (Low State)

STATIC ELECTRICAL CHARACTERISTICS

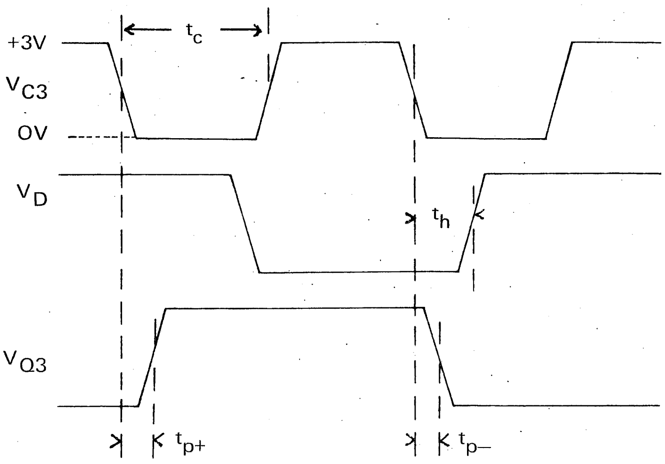
PIN	FUNCTION	PARAMETER (TA = 25°C)	FORCING FUNCTION	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
1	Ground[1] (Common with 8)						
2	Positive[1] supply (Common with 7)	Voltage (V_{CC}) Current	V_{CC} = 5.0V	+4.5 20	5.0 25	5.5 35	V mA
3	Output (Q4) Cell 4	High state current Low state voltage (V_{OL})	VOH = 5.0V I_{LOAD} = 2mA	0 0.25	 0.35	0.01 0.40	mA V
4	Output[2] (Q_3) Cell 3	See (3)					
5	Output (Q_2) Cell 2	See (3)					
6	Output (Q_1) Cell 1	See (3)					
7	Positive supply[1] (Common with 2)	See (2)					
8	Ground[1] (Common with 1)						
9	Data in[1] (D) (Common with 14)	Low state: Voltage V_{IL} Current I_{IL} High state: Voltage V_{IH} Current I_{IH}	VIL = 0V V_{IH} = 5.0V	−0.5 −1.0 2.0 0	−1.4	1.4 −2 5.5 .01	V mA V mA
10	Write clock[3] (C_1) Cell 1	Low state: Voltage V_{IL} Current High state: Voltage V_{IH} Current	V_{IL} = 0V V_{IH} = 5.0V	−0.5 −3 2 0	−4.5	0.8 −5.5 5.5 0.1	V mA V mA
11	Write clock (C_2) Cell 2	See (10)					
12	Write clock (C_3) Cell 3	See (10)					
13	Write clock (C_4) Cell 4	See (10)					
14	Data in[1] (D) (Common with 9)	See (9)					

Notes

1. It is recommended that common pins be externally shorted.
2. Q outputs are non-inverted with respect to D. External pull-up resistors should be used to define the high-state voltage level.
3. On a negative-going clock pulse, the data entry gates are disabled at V_I = 1.4V and data transfer to the store (slave) flip flops is enabled for V_I = 0.8V.



Speed test set-up



Waveforms

TYPICAL SWITCHING PARAMETERS

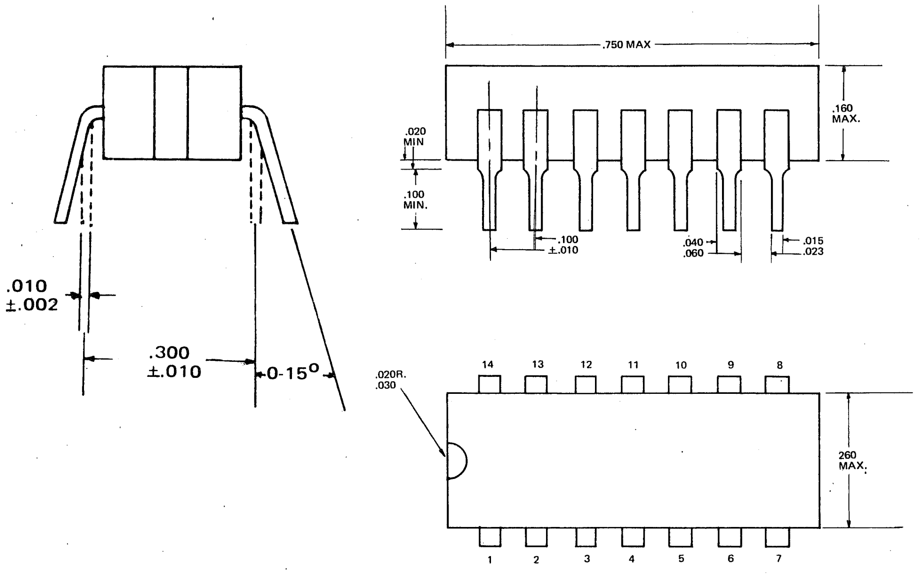
MINIMUM NEGATIVE CLOCK DURATION	t_c	40ns
FULL PROPAGATION TIME	t_p+	40ns
	t_p-	25ns
DATA SET-UP TIME	t_{ds}	35ns
DATA HOLD TIME	t_h	15ns

Figure 4. Switching Characteristics

PIN CONNECTION AND DIMENSIONAL OUTLINE

1. Ground
2. V_{CC}
3. Read Cell 4
4. Read Cell 3
5. Read Cell 2
6. Read Cell 1
7. V_{CC}
8. Ground
9. Data in
10. Write Cell 1
11. Write Cell 2
12. Write Cell 3
13. Write Cell 4
14. Data in

Pins 1-8, 2-7, 9-14
are connected internally



(Dimensions in Inches)

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